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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MARTINEZ, DAVID E	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/928,797	NIE ET AL.	
	Examiner	Art Unit	
	David E Martinez	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

RCE filed

1)☒ Responsive to communication(s) filed on *14 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

1. With regards to claim 1, limitation (f), "the input interface buffer and the output interface buffer being directly addressable by the data processing unit via a separate interface address bus in an independent interface address space", the term via a separate interface address bus is indefinite. It is not clear as to what is being claimed. It is asking for two separate busses, one directly connecting the input port to the data processing unit and the other different bus directly connecting the output port to the data processing unit, these two busses in addition a separate direct address bus connecting the data memory with the data processing unit? Or is it claiming, two separate busses, one bus that connects both input/output ports and the data processing unit together and the other separate bus directly connecting the data memory with the data processing unit? "Via a separate" makes the claim indefinite because it is not clear as to the bus being separate in relation to what, two busses between the two ports or two busses between the two ports and the data memory.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-7, 12-16, 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitter Prior Art (hereinafter referred to as "AAPA") in view of US Patent No. 6,480,929 to Gauthier et al. (Gauthier)

2. In regards to claim 1, AAPA teaches a high speed processor (fig 2) having:

(a) a data processing unit for processing data (fig 2, element labeled "data processing unit" page 2 lines 20,21);

(b) a data memory (fig 2, element labeled "data memory") which is connected to the data processing unit (fig 2, element labeled "data processing unit") via a data bus (fig 2, element labeled "data bus");

(c) at least one input interface buffer (fig 2, element labeled "port in") which is connected to the data bus (fig 2, element labeled "data bus") and has the purpose of buffering input data (page 2 lines 9,10);

(d) at least one output interface buffer (fig 2, element labeled "port out", page 2 lines 24-29) which is connected to the data bus (fig 2, element labeled "data bus") and has the purpose of buffering output data (page 2 lines 24-29);

(e) a ROM memory (fig 2, element labeled "ROM") for storing program data (page 2, lines 22-24), wherein the ROM memory is connected to the data processing unit via lines (fig 2 bus line(s) between elements 44 and 45); and

(f) the input interface buffer and the output interface buffer being directly addressable by the data processing unit via an interface address bus.

The AAPA teaches all that is claimed above, and the data memory and input and output ports all connected to the same address bus, communicating with the data processing unit. AAPA does not disclose the data memory having its own "data memory address bus in a data

address space" to the data processing unit. The AAPA also fails to disclose the input and output interface buffers having their own "interface address bus in an independent interface address space" connected to the data processing unit.

However, Gauthier teaches the use of two independent, separate and distinct address busses by a processor to communicate with two modules. The use of the two different busses allow for address communication to happen concurrently, this allows the a module to get data ready for transmission without much lag after the other module has completed its data transmission. This reduces bus latency and wait states [figs 2A, 2B, elements labeled "DRAM_ADD, ROM_ADD, DRAM_ADD, and FLASH_ADD, see abstract, column 2 lines 10-29, column 3 lines 2-10, column 5, lines 15-25, column 8, line 64 to column 9 line 1 and lines 30-35].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both AAPA and Gauthier to provide two separate independent busses, a "data memory address bus in a data address space", and a "interface address bus in an independent interface address space" because it would allow for concurrent communication on the address busses, thus allowing for reduction in latency and wait states.

3. In regards to claim 2, AAPA teaches a high speed processor (fig 2), wherein the data memory (fig 2, element labeled "data memory") contains at least one RAM memory (fig 2, elements labeled "RAM" page 2, lines 15,16).

4. In regards to claim 4, AAPA teaches a high speed processor (fig 2) according to claims 1 or 2, wherein the data processing unit (fig 2, element labeled "data processing unit") is an RISC data processing unit (page 2 lines 30-35).

5. In regards to claim 5, AAPA teaches a high speed processor (fig 2) according to claims 1 or 2, wherein

the data processing unit (fig 2, element labeled "data processing unit") contains a plurality of addressable internal registers (fig 2, element labeled "R" page 2 lines 20,21).

6. In regards to claim 6, AAPA teaches a high speed processor (fig 2) according to claims 1 or 2, wherein

the data processing unit (fig 2, element labeled "data processing unit") can carry out a plurality of data transfer processor commands in order to directly exchange data between the data memory (fig 2, element labeled "data memory"), the registers (fig 2, element labeled "R") and the interface buffers (fig 2, elements labeled "port in" and "port out")(examples on page 4, lines 9-31).

7. In regards to claim 7-11, 21, AAPA teaches a high speed processor (fig 2), wherein a data transfer processor command is carried out by the data processing unit. The data is loaded from source to target locations. AAPA teaches examples of this on page 4, lines 9-31.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teaching from the AAPA to process data transfer commands from one memory source to another. Memory storage locations are arbitrary and the differences in data transfer commands are dependent only on address specification.

8. In regards to claim 12, AAPA teaches a high speed processor (fig 2), wherein

the input interface buffer (fig 2, element labeled "port in" is connected to an analog/digital converter (fig 2, element labeled "A/D", page 2 lines 6-10).

9. In regards to claim 13, AAPA teaches a high speed processor (fig 2), wherein

the output interface buffer (fig 2, element labeled "port out") is connected to a D/A converter (fig 2, element labeled "D/A", page 2 lines 24-28).

10. In regards to claim 14, it is inherent the data ' processing unit connects to both input and output interface buffers via control lines.

11. In regards to claim 15, AAPA teaches a high speed processor (fig 1 is a black box diagram of fig 2), wherein the input interface buffer is an, xDSL interface buffer for buffering xDSL data (page 1, lines 13-29).

12. In regards to claim 16, AAPA teaches a high speed processor as claimed in claim 15, wherein the xDSL input interface buffer has a data frame detecting device for detecting a data frame synchronization data pattern (while the AAPA may not explicitly teach this, it discloses that it processes predefined data format, page 1 lines 22-32).

13. In regards to claim 20, it is well known in the art wherein processor internal registers have a plurality of memory locations for different data words.

14. In regards to claim 22, AAPA teaches a high speed processor (fig 2), wherein peripherals can be connected to the interface buffers (page 2 lines 6-9, 24-29).
"DQ" and "data sink such as a terminal" are examples taught by the AAPA as peripherals.

15. In regards to claim 23, it is well known in the art to have configurable communication ports.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitter Prior Art (hereinafter referred to as "AAPA") in view of US Patent No. 6,480,929 to Gauthier et al. in further view of US Patent No 5,400,369 to Ikemura.

16. In regards to claims 17, 18, AAPA discloses the high speed processor having a data frame detecting device (can recognize data formats, page 1, lines 22-32) but fails to explicitly disclose the details about the data frame detecting device of claim 16 above.

Ikemura discloses a data frame detecting device having a shift register (fig 2, element 101, column 3 lines 1-5) for writing in input data, a data pattern memory (fig 2, element 102,

column 3 lines 5-15) for storing the data frame synchronization data pattern and a comparator (fig 2 element 102, column 3 lines 5-15) device for bit-by-bit data comparison of the input data written into the shift register, and of the data frame synchronization data pattern stored in the data pattern memory, the comparator device generating a data frame detection signal (column 3, lines 15-20) if the input data written into the shift register is identical to the stored data frame synchronization data pattern;

after the data frame detection signal generated, the shift register is expanded to form a toroidal memory for buffering data (column 6 lines 35-61).

Ikemura discloses the above data frame detecting device to reduce the size of byte and frame alignment circuitry and also to increase the operating speed of byte and frame alignment circuitry (column 1, lines 55-60).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the teachings of ikemura to the combination of AAPA and Gauthier, in order to reduce the size of the circuitry and increase the operating speed.

In regards to claim 19, it is well known in the art to output modulated data such as PCM data through a medium. It would have been obvious to have the output interface buffer be a PCM interface buffer for buffering PCM data.

Response to Arguments

Applicant's arguments filed on 9/14/04 have been fully considered but they are not persuasive.

Applicant argues that "Gauthier does not disclose or suggest input and output interface buffers which are connected to a data bus and have the purpose of buffering input and output data respectively as recited by elements (c) and (d) of claim 1." (Remarks page 10) and that "Gauthier does not disclose or suggest the features recited in elopement (f) of claim 1"

Examiner respectfully disagrees. Examiner relies on the input/output interface buffers disclosed by AAPA to make the rejection in combination to what Gauthier teaches, which is the use of two **separate** address busses to communicate to two different modules. This teaching is what is being applied to the AAPA for the benefit shown above under the claim 1 rejection and also in the cited parts of Gauthier's reference. Gauthier's reference constitutes competent prior. Gauthier shows two separate address busses connected to two separate memory elements 202 and 200. Gauthier's separate address busses can be implemented with AAPA to come to the claimed invention since the input/output ports are interface buffers (memory elements) thus they are able to be used with Gauthier's separate address busses.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E Martinez whose telephone number is (571) 273-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (571) 272-4146. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DEM

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